REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1, 3 through 5, 10, 15, 19, 22, and 43 through 50 are now in this case. Claims 1, 3, 22, and 48 are amended. Claims 49 and 50 are newly added. Claims 6 through 8, 16, 20, and 21 are newly canceled.

Claims 1, 3 through 6, 8 through 10, 15, 16, 19, 20, 22, and 43 through 45 stand rejected under §102(e) as anticipated by the Miyauchi reference[1]. Claims 7 and 21 stand rejected under §103 as unpatentable over the Miyauchi reference in view of the Kramer reference.[2]

Claim 1 is amended to advance the prosecution of this case by clarifying its distinction over the Miyauchi reference. Amended claim 1 now recites that the non-volatile memory is of the MLC NAND type.[3] The writing step following the writing of the contents of a first logical sub-unit is amended to now recite the writing of contents of a third logical sub-unit into a third programming unit of the first group, where this third programming unit is later in the sequence of programming units than first and second programming units, and where the third logical sub-unit is later in the sequence of logical sub-units than first and second logical sub-units.[4] The last writing step of the claim now requires the writing of contents of a second logical sub-unit, earlier in the sequence of logical sub-units than the third logical sub-unit, into a programming unit in a second group of programming units of the first erase unit.[5] No new matter is presented by this amendment to claim 1, given its clear support in the specification.

Claims 6 through 8 are canceled, considering the amendment to claim 1. Claim 3 is amended for consistency with amendment to claim 1, upon which it depends.

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[1] U.S. Patent No. 6,430,650 B1, issued August 6, 2002 to Miyauchi, from an application filed June 17, 1996.

[2] U.S. Patent No. 6,182,239 B1, issued January 30, 2001 to Kramer.

[3] As previously recited in claim 7, now canceled along with claim 6.

[4] *See* specification of S.N. 10/679,008, *as published as* U.S. Patent Application Publication No. US 2004/0103241 A1, paragraphs [0046] through [0050].

[5] *Id.*

New claim 49 is added to more completely cover all aspects of Applicants' invention. Specifically, claim 49 further requires, relative to amended claim 1 upon which it depends, that the contents of the second logical sub-unit are written into the second programming unit of the second group of programming units, where the second programming unit is between the first and third programming units in that second group. The specification clearly supports this new claim,[6] and as such no new matter is presented by this amendment.

The method of amended claim 1 and its dependent claims provides important advantages over the prior art, including the Miyauchi and Kramer references of record in this case. In particular, the inventive method enables out-of-sequence write operations to be performed in an MLC NAND flash memory, in which out-of-sequence writes are otherwise prohibited, without consuming another erase unit, or physical block, to do so.[7] This not only improves the flexibility and performance of writing data in this important and widely-used type of flash memory, but also reduces erase wear in such devices.

Applicants submit that amended claim 1 and its dependent claims are novel and inventive over the Miyauchi and Kramer references, as well as the other prior art of record in this case.

First, the Miyauchi reference nowhere discloses that its non-volatile memory is an MLC NAND flash memory, as required by amended claim 1.[8]

Secondly, the Miyauchi reference nowhere discloses or suggests the sequence of writing operations required by amended claim 1. This lack of disclosure is made evident by its flow charts of Figures 7A and 7B, and the accompanying description. According to the Miyauchi reference, decision S103 of Figure 7A determines whether a physical group number is "registered" (*i.e.,* mapped) to the logical group number to which data is to be written.[9] If so (decision S103 is YES), decision S117 is then performed to determine whether the destination sector in that group is used; if not (decision S117 is NO), data is written to the sector in process

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[6] Specification, *supra,* paragraphs [0046] and [0050].

[7] Specification, *supra,* paragraphs [0009] through [0011], [0050], [0077].

[8] And as admitted in the Office Action of August 9, page 20.

[9] Miyauchi, *supra,* column 6, lines 7 through 32.

S118.[10] In this case, data is written to that destination sector regardless of the position of that sector relative to sectors in that group that have previously been written. In other words, according to the Miyauchi reference, data will be written to the unused destination sector even if a later sector in that very group has already been written.

In contrast, the method of amended claim 1 requires, after a third programming unit in a first group within an erase unit has been written with contents of a third logical sub-unit (later in sequence than a second logical sub-unit), the writing of contents of a second logical sub-unit into a programming unit in a second group of programming units in that same erase unit. This writing step is not disclosed by, and would not be performed, under the Miyauchi reference – rather, according to the reference, these contents would be written into the second sector of the first group, via decision S117 and process S118.

Accordingly, Applicants submit that amended claim 1 and its dependent claims are novel over the Miyauchi reference, because the reference fails to teach the third writing step of amended claim 1, nor does it disclose that the memory is an MLC NAND flash memory as is also required by amended claim 1.

Furthermore, Applicants submit that one skilled in the art would not obviously arrive at the method of amended claim 1, given the teachings of the Miyauchi and Kramer references, or the other prior art of record in this case.

As mentioned above, the method of amended claim 1 is directed to an MLC NAND flash memory, in which out-of-sequence write operations are prohibited.[11] While the Kramer reference teaches that MLC NAND flash memories are known, it nowhere provides any teaching or suggestion of the grouping of programming units within an erase unit into a plurality of blocks, much less the writing steps required by amended claim 1. Accordingly, the combined teachings of these two references, even if such combination is suggested (which it is not) fall short of the requirements of amended claim 1. Nor do the other references of record in this case provide such teachings.

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[10] Miyauchi, *supra,* column 6, lines 29 through 32, and lines 56 through 61.

[11] *See* specification, *supra,* paragraph [0009] through [0011].

Applicants further submit that there is no suggestion to combine the Miyauchi and Kramer references, and then to modify that combination in such a manner as to reach amended claim 1. First, the skilled reader would not be motivated to combine these two references in the first place, because the combination would not be operable. As mentioned above, it is well known in the art that MLC NAND flash memories prohibit out-of-sequence write operations. However, the Miyauchi reference expressly teaches the performing of out-of-sequence writes within a single block, or erase unit. Accordingly, there is no way in which the operations disclosed by the Miyauchi reference can be operably implemented within an MLC NAND flash memory. The suggestion is further negated by the nature of the Kramer flash memory, which is disclosed as being a "sequential access memory device[]" rather than a "random access memory"; indeed, a memory that supports "only sequential access".[12] Accordingly, the non-sequential write operations disclosed by the Miyauchi reference could not be used in connection with the Kramer flash memory. This inoperability of the combination of the Miyauchi technique with the Kramer flash memory negates any suggestion to combine their teachings in such a manner as to reach amended claim 1.

Furthermore, as noted above, the combined teachings of these references fall short of the requirements of amended claim 1. Applicants further submit that there is no suggestion to modify these teachings in such a manner as to reach amended claim 1, and submit that the necessary modification would be beyond the ordinary creativity of the skilled artisan at the time of this invention. This substantiality of the differences between the properly combinable teachings of the prior art and the method of amended claim 1 is borne out by the important advantages of this invention in allowing out-of-sequence write operations in an MLC NAND memory, in such a manner as to reduce the erase wear on the device. Especially considering that these advantages stem directly from the differences between the claims and the prior art, Applicants submit that these advantages further support the patentability of amended claim 1 and its dependent claims.

Applicants therefore submit that amended claim 1 and its dependent claims are not only novel, but are patentably distinct over the prior art of record in this case.

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[12] Kramer, *supra,* column 5, lines 52 through 63.

Claim 22 is similarly amended as claim 1, discussed above. Specifically, Claim 1 is amended to advance the prosecution of this case by clarifying its distinction over the Miyauchi reference. Amended claim 1 now recites that the non-volatile memory is an MLC NAND flash memory, and that the programming units within each erase unit are arranged in a sequence including first, second, and third programming units. The means for controlling the writing of contents does so according to a sequence of operations that comprise writing the contents of a third logical sub-unit into a third programming unit of the first group, the third programming unit later in the sequence of programming units than first and second programming units, and writing contents of a second logical sub-unit, earlier in the sequence of logical sub-units than the third logical sub-unit, into a programming unit in a second group of programming units of the first erase unit. This amendment to claim 22 is supported in the same manner as discussed above relative to amended claim 1, and as such no new matter is presented.

Claims 16, 20, and 21 are canceled because of the amendment to claim 22. Claim 48 is amended to correct a minor error in its preamble regarding its dependency.

New claim 50 is added to more completely cover all aspects of Applicants' invention. Similarly as claim 49 discussed above, claim 50 further requires, relative to amended claim 22, that the operation of writing contents of the second logical sub-unit writes those contents into the second programming unit of the second group of programming units, where the second programming unit is between the first and third programming units in that second group. No new matter is presented by the addition of this new claim.

The system of amended claim 22 and its dependent claims provides similar advantages over the prior art as does the method of amended claim 1, discussed above. In short, these advantages include the ability to perform out-of-sequence write operations in an MLC NAND flash memory in which out-of-sequence writes are otherwise prohibited, while reducing erase wear.

For similar reasons as discussed above, Applicants submit that amended claim 22 and its dependent claims are novel and inventive over the Miyauchi and Kramer references and the other prior art of record in this case.

Amended claim 22 requires an MLC NAND flash non-volatile memory. This type of memory is not disclosed by the Miyauchi reference,[13] rendering amended claim 22 novel over the reference.

Furthermore, the Miyauchi reference nowhere discloses or suggests the sequence of writing operations performed by the controlling means of amended claim 22. As discussed above, Figures 7A and 7B and the corresponding description of the Miyauchi reference illustrate an out-of-sequence write operation, in which a sector in a previously written-to group is then written to regardless of its position within that group (*i.e.,* regardless of whether a later sector in that group has previously been written).[14] In contrast, the controlling means of amended claim 22 operates to write contents of a second logical sub-unit into a programming unit in a second group of programming units in that same erase unit, once a third programming unit in the first group has been written. This operation is not disclosed by the Miyauchi reference, nor would it be performed according to the reference. Instead, the operation of writing the second logical sub-unit after writing the third logical sub-unit would, according to the Miyauchi reference, write those contents into the second programming unit of the first group, and not into the second group as claimed.

Accordingly, Applicants submit that amended claim 22 and its dependent claims are novel over the Miyauchi reference.

Furthermore, Applicants submit that amended claim 22 and its dependent claims are patentably distinct over the prior art, because the skilled artisan would neither combine the Miyauchi and Kramer references, nor modify those teachings and those of the other prior art of record, in such a manner as to reach amended claim 22.

As discussed above, the Kramer reference teaches an MLC NAND flash memory, albeit such a flash memory that is a “sequential access memory device[]”that supports “only sequential access”, rather than a “random access memory”.[15] In such an MLC NAND flash memory, as discussed above, out-of-sequence write operations are not permitted.[16] As a result, the skilled reader would not be motivated to combine the Kramer reference with the Miyauchi reference, because the operations described by the Miyauchi reference would not be operable in the Kramer MLC NAND flash memory. As noted above, the Miyauchi reference describes an out-of-sequence write operation. There is no way that such a write operation could be performed in the sequential-access flash memory of Kramer, nor in any MLC NAND flash memory, in which out-of-sequence writes are not permitted. This inoperability of the combination negates any suggestion to combine their teachings in such a manner as to reach amended claim 22.

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[13] And as admitted in the Office Action of August 9, page 20.
[14] Miyauchi, *supra,* column 6, lines 7 through 32, lines 29 through 32, and lines 56 through 61.
[15] Kramer, *supra,* column 5,lines 52 through 63.

Nor is there any suggestion to modify the properly-combinable teachings of these two references, nor any other reference of record, so as to reach amended claim 22. Such modification is not only not suggested, but would require more than the ordinary creativity of the skilled artisan at the time of this invention. The important advantages resulting from the differences between the claim and the prior art further support the patentability of this inventive system.

Applicants therefore submit that amended claim 22 and its dependent claims are novel and patentably distinct over the prior art of record in this case.

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[16] Specification, *supra,* paragraph [0009] through [0011].

For these reasons, Applicants respectfully submit that the claims now in this case are in condition for allowance. Favorable reconsideration of this application in light of this amendment is respectfully requested.

Respectfully submitted,

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